A FET AMPLIFIER IN FIN-LINE TECHNIQUE+

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ABSTRACT

This paper describes the successful demonstration of a stable FET amplifier using fin-line technique. The circuit has been realized in integrated E-plane technology, utilizing two main fin-line ports and a microstrip/coplanar bias circuit. The amplifier was designed for 17 GHz operation using a NE67300 FET and achieved a gain of 6 dB over a bandwidth of 1 GHz.

INTRODUCTION

It can be seen from previous publications that much effort has been expended in deriving a circuit configuration suitable for mounting FETs in fin line technique. Such a mounting structure would enable the realization of FET low noise amplifiers and oscillators in fin line thus making possible completely integrated low noise receivers in fin line or E-plane technique.

Previous efforts at realizing an amplifier in E-plane technique involved employing an E-plane transition from waveguide to a FET device mounted in microstrip [1]. Absorbent material was placed at various points on the circuit as a means of stabilizing the device at frequencies below the cut-off frequency of the waveguide. Losses due to the transitions and absorbent material make this approach unattractive for use in an integrated fin line receiver.

Oscillator circuits using FETs in fin line were published by Jacob and Ansorge [2] and Meinel [3]. These circuits utilized either a cross-shaped or T-shaped arrangement of unilateral fin lines with the device mounted at the junction of the slots. Owing to the unpredictable coupling between the lines connecting the input and output terminals of the device, the designs of these oscillators were largely empirical. In addition, no provision for low frequency stabilization of the FET device was provided.

This paper presents a novel circuit configuration for mounting a FET in fin line. It allows the design of an unconditionally stable amplifier without the use of lossy waveguide-to-microstrip transitions or absorbent material. Other circuit types such as FET oscillators or mixers may also take advantage of the novel mounting structure proposed here.

The RF Circuit

The waveguide housing is a split block type consisting of two parallel rectangular waveguides sharing a common broad wall (septum). The waveguides are isolated from each other, except for a small window in which the transistor is mounted (see Fig. 1). The input of the amplifier begins with a conventional rectangular waveguide that tapers into a single fin, unilateral fin line, to which the gate of the transistor is connected (see Fig. 2). The transistor is installed in an opening in the septum, and the drain lead is bonded to an identical fin in the output waveguide. Fin line short circuits terminate the input and output lines a quarter wavelength beyond the FET terminals, thus presenting an open circuit to the transistor. The source pads of the FET chips are bonded to the printed circuit.

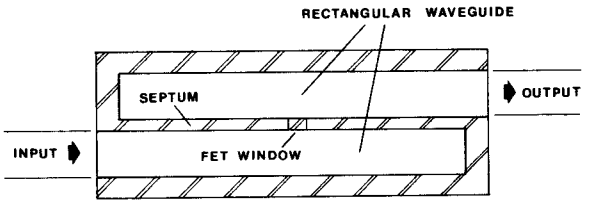

FIGURE 1 SPLIT BLOCK HOUSING

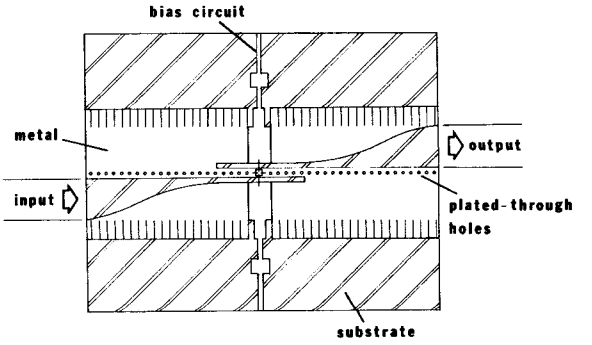

FIGURE 2 METALIZATION PATTERN OF FIN LINE AMPLIFIER

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The circuit is printed on a 0.010 inch thick RT/Duroid substrate (ε_r = 2.22). In order to prevent any RF coupling between the two waveguide structures through the substrate, a series of plated-through holes is used as a shield along the common broad wall junction. The isolation between the input and output ports, without transistor, was increased to greater than 30 dB with the plated-through holes (Fig. 3).

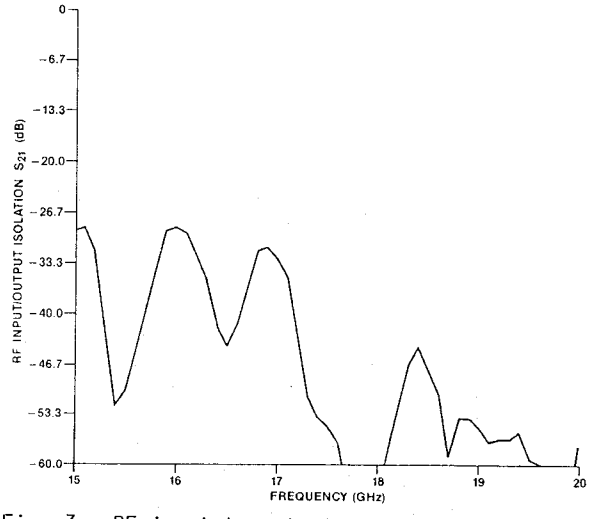


Fig. 3. RF input-to-output isolation of circuit without transistor.

The Bias Circuit

A special bias circuit was designed to present a good match to the transistor at lower frequencies where the FET is potentially unstable and the fin line structure is cut off. In addition, the bias circuit was designed to be transparent to the RF. The bias line begins at the FET terminals, with a coplanar waveguide made from two series slots in the fin (see Fig. 4). Each slot is one half wavelength long at RF and runs from the broadwall to the edge of the fin in order to reflect a short in series with the fin line slot.

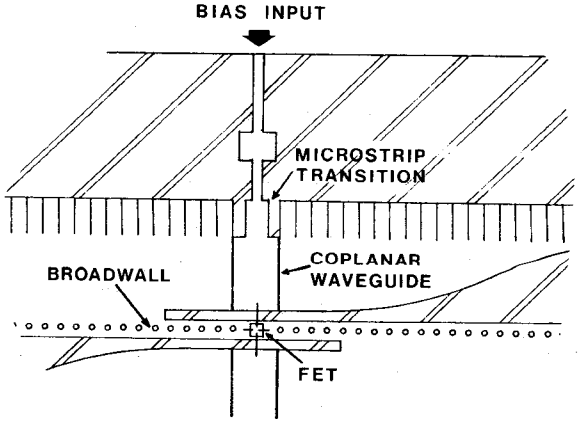


FIGURE 4 DETAILS OF BIAS CIRCUIT

At the outer broadwall plane, the coplanar line makes a transition to microstrip line that continues on to a matched load (50 Ω) through a bias tee. A filter is used to reduce RF leakage through the microstrip. Since the bias circuit is comprised of microstrip and coplanar waveguide, a low (50 Ω) impedance can be presented to the FET terminals at all frequencies from D.C. to the cut-off of the filter.

A plot of measured RF leakage, from one of the waveguide ports through the bias circuit is presented in Fig. 5. From this graph, it may be seen that the leakage is least around 15.2 GHz and begins to increase for higher frequencies. At the design frequency the leakage is approximately -27 dB. This was considered a reasonable value for our experiment.

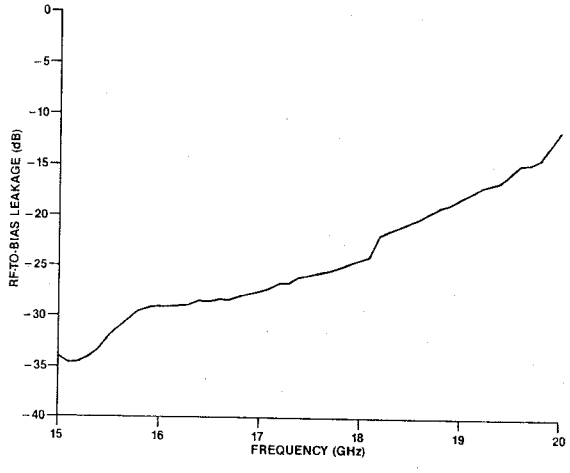
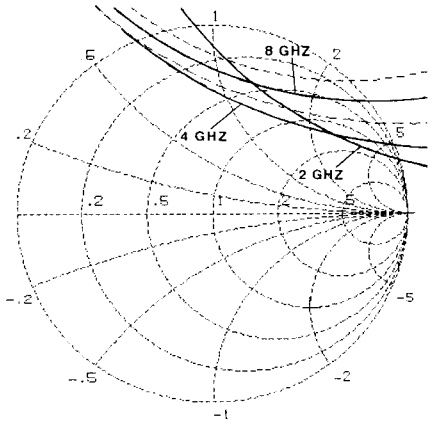


Fig. 5. Leakage from waveguide port to bias port.

For the FET device selected for this work (NE67300), the most critical potentially-unstable region is situated in the neighborhood of 4 to 5 GHz as shown in Fig. 6. Thus, the bias circuit was designed to have a low S_{11} in that critical frequency region. To verify the performance of the bias circuit, the FET was replaced by a 50 Ω chip resistor and the reflection coefficient was measured at the microstrip bias input line. The circuit showed a better than required match for all frequencies especially from 3.5 to 5.6 GHz, where S_{11} was less than -18 dB (see Fig. 7.).



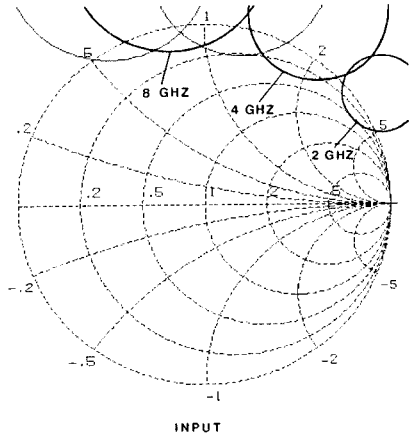


FIGURE 6 NE67300 STABILITY CIRCLES

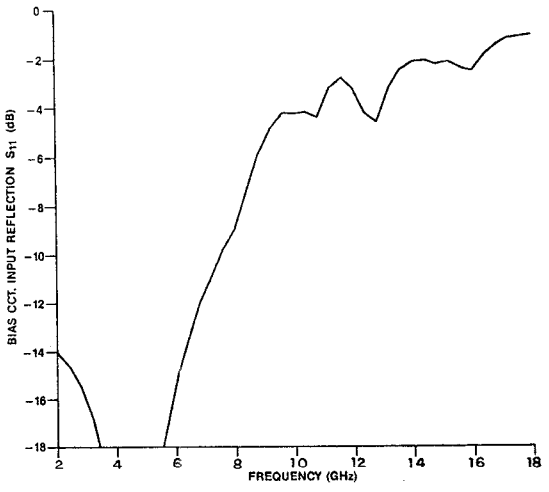


Fig. 7. Input reflection coefficient of bias circuit.

Amplifier Performance

A photograph of the complete amplifier, showing the circuit substrate and housing, is displayed in Fig. 8. The transistor was matched using short-circuited series stubs at both input and output ports. The stubs were designed using data given in [4] and were tuned using silver paint to adjust the length. Tuning was performed directly during measurement through an opening or window in the sidewall of the housing situated above the transistor. After tuning, the window was closed using a brass cover. Since most of the fields are concentrated in the slot of the fin line, the opening had no significant effect on the response of the circuit and tuning was performed easily.

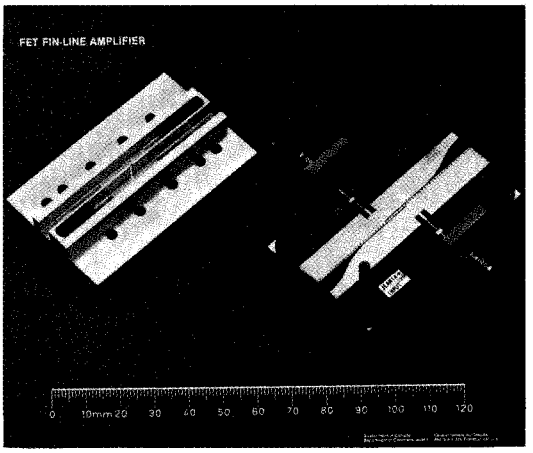


Fig. 8. Photograph of Fin Line FET Amplifier.

The final amplifier displayed unconditional stability over all frequencies. The gain was greater than 6 dB over a 1 GHz bandwidth centered at 16.8 GHz (see Fig. 8). The measured noise figure was 3.5 dB at that frequency.

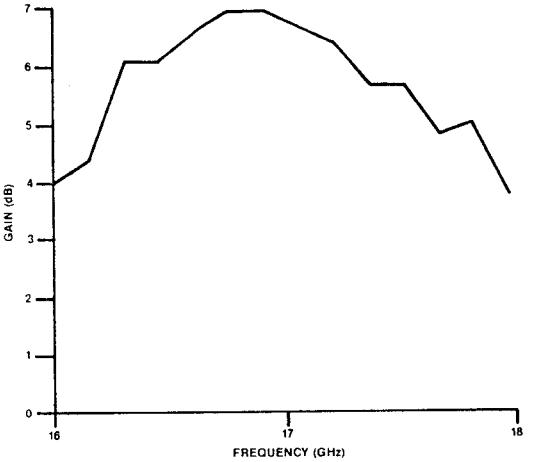


Fig. 9. Measured gain of fin line amplifier.

CONCLUSION

To this date, an unconditionally stable FET amplifier mounted in fin line has not been reported in the open literature. This paper presents a novel approach to achieving stable amplification using FETs in fin line. Stabilization is achieved by use of a unique coplanar/microstrip bias circuit while RF performance is maintained by decoupling the input and output fin lines using a combination of novel approaches including plated-through holes.

A useful amplifier having 6 dB gain and 3.5 dB noise figure over a 1 GHz bandwidth at 17 GHz was designed. This result will encourage further effort in this area to produce multi-stage amplifiers and complete integrated receivers in fin line using FETs. Also, other components such as FET oscillators and mixers may take advantage of the stabilizing and isolating properties of this circuit configuration.

ACKNOWLEDGEMENT

The authors are grateful to P. Deegan for assistance in mechanical design and construction of the housing. Also the helpful discussions and technical assistance of B. Clarke and G. Boucher are gratefully acknowledged.

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